Comp 3725 Nov. 17/12

From serial execution to Parallel Execution,
↳ non-overlapped ↳ instruction overlapping
↳ instruction pipelining

Note: Data Pipelining will be considered later.

Non-overlapped Instruction Execution: An instruction completes all the stages of execution before the next instruction begins.

eg. MIPS using a serial machine.

$I_1 \rightarrow$ IR | ID | Ex | Mem | WB $\rightarrow I_2 \rightarrow$ IR | ID | Ex | Mem | WB

Each step takes equal amount of time.

In MIPS each stage = 10ns (minor cycle)

Total amount of time to evaluate

1 instruction = # of states * minor cycle

in MIPS: 1 inst = 5 * 10ns = 50ns

$T(s)$ = Time to execute s instructions.

$= s * m * t$ (# of inst * # of stages * minor cycles)

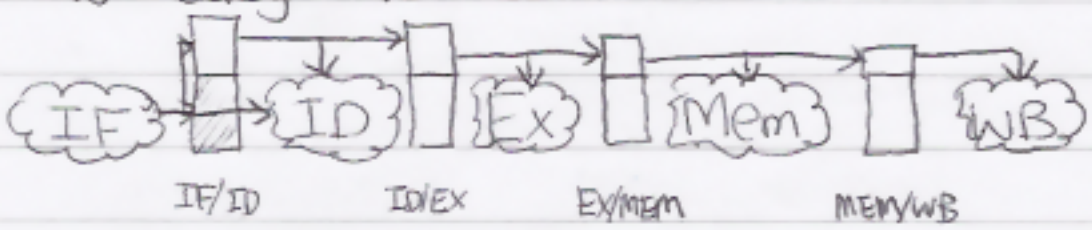
Pipelined Machine

Motivation: In serial execution when a particular instruction is in 1 stage all the other stages are remaining idle, hence it is inefficient.

idea: To 'push' instruction stream through the stages and obtain finished instructions from the last cycle.

Two important issues for pipeline execution:
① Managing control signals for the "traveling" instructions through each stage.
② Dependency issues among instructions
  a) Resource dependency among stages
    eg. MIPS: WB and ID use same common hardware
  b) Data dependency among instructions
    eg. I_1: $R_1 \leftarrow R_2 + R_3$
      I_2: $R_4 \leftarrow R_1 + R_3$
  c) Control dependency among instructions
    eg. I_2: If $(R_2 = R_1)$ Then $PC \leftarrow PC + 4 + 100$
      I_3: ~~~~

Problem 1 is easy to solve.
eg. MIPS

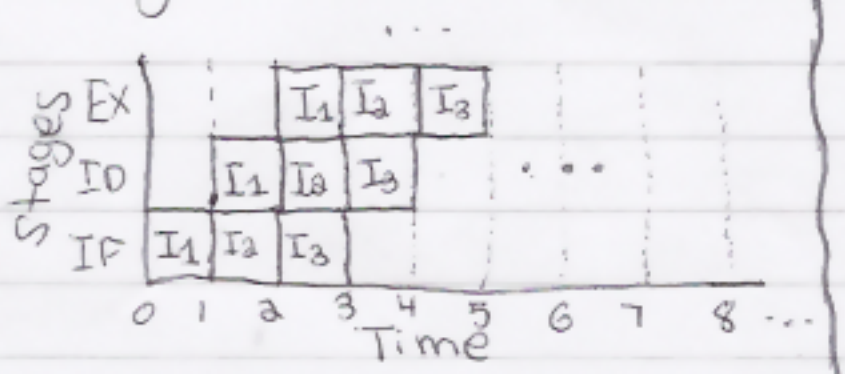


The control signals are stored in the buffer memory to travel along the pipeline.

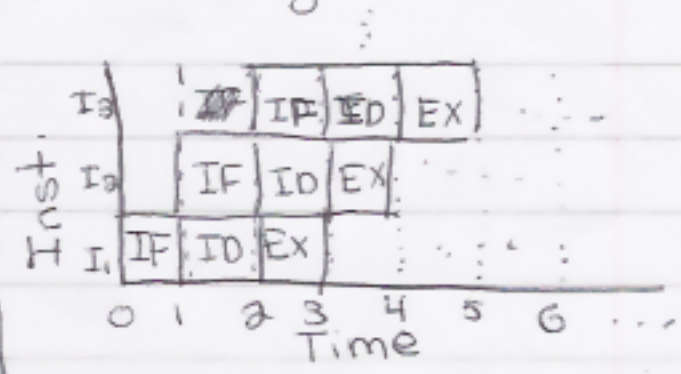
IDEAL OVERLAP (ONLY R-Type Instructions, No LW/SW Type, No Branch, No Data Dependence, No Resource Dependency)

Timing Diagrams Two Styles: 1) Gnatt Diagram 2) Hennessey-Pattsson Diagram

Gnatt Diagram



HP Diagram



Calculating Execution Time for <u>Ideal Overlap</u>

$$T_{P\,(IDEAL)} = ((M-1) + N)t$$

(M-1): bubbles; N: one inst/cycle

M = # of Stages
N = # of Instructions
t = clock cycle

$$\text{Speed-up Ratio} = \frac{T_S}{T_P} \quad \begin{matrix}(\text{Time of serial}) \\ (\text{Time of pipelined})\end{matrix}$$

$$\therefore \frac{M*N*t}{(M-1+N)*t}$$

If $N \gg M$ Then Speed-Up Ratio $\rightarrow M$