Comp. 3725 Jan. 11/12

Genen's IPC

IPC with a bit more specifics.

```
REPEAT
  C1: IR ← IM[PC]      //Instruction fetch
  C2: PC ← PC+4        //Sequential implementation of PC
  C3: OP ← DC(IR)      //Calculate op code
  C4: OPRs ← IA(IR)    //Calculate operands
  Case OP Of                                   } execute state
  C5: Add: OPR1 ← OPR2 + OPR3
  C6: Lw: OPR1 ← DM[OPR2 + OPR3]
  C7: Sw: DM[OPR2 + OPR3] ← OPR1
  C8: J: PC ← OPR1
  C9: Beq: If (OPR1 = OPR2) Then PC ← PC+4 + 4*OPR3
  End Case
Goto Repeat
```

Legends: PC - Program Counter
IR - Instruction Register
IM - Instruction Memory
DC - Opcode Decoder
OP - Decoded Opcode
IA - Operand Calculator
OPRs - Actual Operand(s) - OPR_1, OPR_2, OPR_3
DM - Data Memory

IPC is written using RTL (HDL)
↓ Hardware Design
① Labels are used as control signals
② Control Unit mimics the flow of controls of the IPC: FSM → PLA (Automatic/Systematic)
③ The other section: Static architecture is a collection of all the registers, arrays (memory), functional units